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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/703,034
Filing Date: October 31, 2000
Appellant(s): ZBICIAK, JOSEPH R.

Zbiciak
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04/23/2008 appealing from the Office action mailed 08/07/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,167,419	Saishi et al.	12-2000
6385634	Peleg et al.	05-2002
2003/0088601 A1	Pitsianis et al.	05-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

A. Claim 28 was rejected under 35 U.S.C. 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

B. Claim 13 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al. (U.S. Patent No. 6,167,419) and Pitsianis et al. (U.S. Patent Application Publication No. 2003/0088601).

C. Claims 25-27 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al. (U.S. Patent No. 6,167,419) and Peleg et al. (U.S. Patent No. 6,385,634).

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 28, the limitations "said first Q shifter…specified number of bits" in lines 6-7 and "said second Q shifter shifting…specified number of bits" in lines 10-12 are unclear since these limitations are unclear as incomplete. For examination purposes, the examiner considers the first limitation as "said first Q shifter shifting said first product by specified number of bits in response to the rounding dot product instruction" and the second limitation as "said second Q shifter shifting said second product by specified number of bits in response to the rounding dot product instruction instruction".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saishi et al. (U.S. 6,167,419) in view of Pitsianis et al. (U.S. Patent Application Publication No. 2003/00088601).

Re claim 13, Saishi et al. disclose in Figures 5-9 a digital system having a microprocessor (e.g. col. 1 lines 5-10 for processing digital signals) operable to execute a rounding product instruction (e.g. abstract and Figure 5 wherein the product is output of

multiplication 505 and the rounding is done by rounding signal 514), wherein the microprocessor comprises: storage circuitry for holding pairs of elements (e.g. Figure 5 and Figure 8 wherein storage is used to hold the multiplier and multiplicand for input into the multiplication means 503); a multiply circuit (e.g. multiplication means 503 in Figure 5, in particular the multiplier for generating subproducts 505) connected to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the product instruction (e.g. the multiplication means 503 is used to multiply the multiplier and multiplicand as pairs of elements together in Figure 5), the multiply circuit (e.g. multiplication means 503 in Figure 5 or Figure 8 for generating multiplication result 803) comprising a plurality of multipliers equal to the first number of pairs of elements (e.g. multiplication means in Figure 5 as single multiplication means corresponding to single pair of elements multiplier 501 and multiplicand 502 in Figure 5); an adder/subtractor circuit (e.g. an adder means including components 506-508 in Figure 5) having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers (e.g. inputs 505 as subproducts of multiplications between multiplier 501 and multiplicand 502 in Figure 5) and a mid-position carry (e.g. rounding signal 515 in Figure 5) input to a predetermined bit (e.g. predetermined bit is predetermined rounding position 805 in Figure 8 and col. 8 lines 15-17) for mid-position rounding (e.g. wherein the mid-position rounding is set when the rounding position is set at mth rounding position as seen in Figure 8) responsive to the rounding product instruction (e.g. abstract and Figure 5 wherein the product is output of multiplication 505 and the rounding is done by rounding

signal 514 and component 512 in Figure 5); and a shifter (e.g. components 510 and 520 in Figure 5) connected to receive an output of the adder/subtractor circuit (e.g. multiplication with rounding signal added 509 in Figure 5), the shifter operable to shift a selected amount in response to the rounding product instructions (e.g. corresponding to instruction control means 512 in Figure 5).

Saishi et al. fail to disclose in Figures 5-9 product instruction is the dot product instruction for multiplying multiple pairs of elements. However, the dot product instruction for multiplying multiple pairs of elements is well known in the art of technology as addressed in Pitsianis et al.'s invention. Pitsianis et al. disclose in Figure 3B and 6 the dot product instruction for multiplying multiple pairs of elements wherein the dot product instruction is an instruction for performing complex multiplication as seen in Figures 3B and 9. In extension, the dot/complex product instruction for performing multiplication between multiple pars of elements is seen in Figures 3B or 6 wherein it discloses the fetching a first pair of elements (e.g. Xr and Yi in 603 and 605) and a second pair of elements (e.g. Xi and Yr in 603 and 605); forming a first product (e.g. result 617 as Xr*Yi) of the first pair of elements and a second product (e.g. result 619 as Xi*Yr) of the second pair of elements; combining (e.g. component 625 for adding) the first product with the second product; form a combined product as result (e.g. output of 625 as result of addition or output of 623 as result of subtraction of sub-products).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a dot product operation for multiplying multiple pars of elements as seen in Pitsianis et al.'s invention into Saishi et al.'s invention

because it would enable to efficiently compute the sum of products inwhich would be used in many practical applications (e.g. FFT as seen in abstract and paragraphs [0002-0005] in column 1).

5. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saishi et al. (U.S. 6,167,419) in view of Peleg et al. (U.S. 6,385,634).

Re claim 25, Saishi et al. disclose in Figures 5 and 9 a data processing apparatus (e.g. Figure 5 and col. 1 lines 5-10 for processing digital signals in image and sound processing fields) comprising: a first multiply circuit (e.g. multiplication means 503 in Figure 5) having first and second inputs and an output (e.g. multiplier 501 and multiplicand 502 as inputs and subproducts 505 as output in Figure 5), said first multiply circuit operable in response to a product instruction to multiply data received at said first and second inputs (e.g. multiplier 501 and multiplicand 502) and generate a first product at said output (e.g. output of component 504 as subproducts 505 in Figure 5); an adder/subtractor circuit (e.g. components 506-508 as adder for adding inputs in Figure 5) having first and second inputs (e.g. output of component 504 as subproducts 505 in Figure 5), a mid-position carry input (e.g. rounding signal 515 in Figure 5) to a predetermined bit (e.g. predetermined bit is predetermined rounding position 805 in Figure 8 and col. 8 lines 15-17) and an output (e.g. output of component 508 in Figure 5), said first input receiving said first product from said first multiply circuit (e.g. plurality of subproducts 505 in Figure 5), said adder/subtractor circuit (e.g. components 506-508 in Figure 5) operable in response to said product instruction to arithmetically combine said

first and second products and a "1" input at said mid-position carry input of said predetermined bit thereby forming a mid-position rounded sum (e.g. the combination is performed at component 506 in Figure 5 and arithmetic representation is seen in Figure 8); and a shifter (e.g. components 510 and 520 in Figure 5) connected to receive an output of the adder/subtractor circuit (e.g. multiplication with rounding signal added 509 in Figure 5), the shifter operable to shift a selected amount in response to the rounding product instructions (e.g. corresponding to instruction control means 512 in Figure 5).

Saishi et al. fail to disclose the dot product instruction having a second multiply circuit having first and second inputs and an output, said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output; and an adder/subtract is receiving said first and second product from said first and second multiply circuits respectively. However, Peleg et al. discloses in Figures 1 and 8 the dot product instruction (e.g. packed instruction set 140 in Figure 1 and col. 17 line 49 to col. 19 line 33) having a second multiply circuit having first and second inputs and an output (e.g. multipliers 810-813 in Figure 8 wherein each of multiplier multiplies pair of corresponding elements to yield corresponding product), said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output (e.g. let say output of multiplier 810 as first product of first multiplier and multiplier 811 as second product of second multiplier in Figure 8); and an adder/subtract (e.g. component 850 in Figure 8) is receiving said first and second product from said first and second multiply circuits respectively (e.g. Figure 8).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the dot product instruction having a second multiply circuit having first and second inputs and an output, said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output; and an adder/subtract is receiving said first and second product from said first and second multiply circuits respectively as seen in Peleg et al.'s invention into Saishi et al.'s invention because it would enable to efficiently compute the sum of products inwhich would be used in many practical applications (e.g. col. 17 lines 49-60 and col. 19 lines 25-33).

Re claim 26, Saishi et al. disclose arithmetic combination of subproducts is an arithmetic sum (e.g. component 506 in Figure 5).

Saishi et al. fail to disclose the arithmetic combination of said first and second products. However, Peleg et al. disclose the arithmetic combination of said first and second products as sum (e.g. Figure 8).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the arithmetic combination of said first and second products as sum as seen in Peleg et al.'s invention into Saishi et al.'s invention because it would enable to efficiently compute the sum of products inwhich would be used in many practical applications (e.g. col. 17 lines 49-60 and col. 19 lines 25-33).

Re claim 27, Saishi et al. fail to disclose dot product instruction is a dot product with negate instruction; and said arithmetic combination of said first and second products is a difference of said second product from said first product in response to said dot

product with negate instruction. However, Peleg et al. disclose dot product instruction is a dot product with negate instruction (e.g. packed instruction set 140 in Figure 1); and said arithmetic combination of said first and second products is a difference of said second product from said first product in response to said dot product with negate instruction (e.g. Figure 8 with subtraction is set).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add dot product instruction is a dot product with negate instruction; and said arithmetic combination of said first and second products is a difference of said second product from said first product in response to said dot product with negate instruction as seen in Peleg et al.'s invention into Saishi et al.'s invention because it would enable to efficiently compute the sum of products inwhich would be used in many practical applications (e.g. col. 17 lines 49-60 and col. 19 lines 25-33).

(10) Response to Argument

A. Claim 28 was rejected under 35 U.S.C. 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The applicant comments in page 7 third paragraph for claim 28 rejected under 35 U.S.C. 112 that the amendment after final rejection submitted October 8 2007 would overcome the rejection for this claim in previous Office action. In addition, the examiner indicated the amendment would be enter but failed to state whether this amendment cured this rejection.

The examiner respectfully submits that the applicant did not explicitly state/request the reason why the amendment after final rejection would overcome the rejection of claim 28 under 35 U.S.C. 112. Thus, the examiner did not necessary need to provide the statement whether the amendment would overcome the rejection of claim 28 under 35 U.S.C. 112. In general, the amendment after final rejection submitted October 8 2007 did not address/cure the rejection since the unclear issue still exists within the claim 28, particularly the limitations "said first Q shifter…specified number of bits" in lines 6-7 and "said second Q shifter shifting…specified number of bits" in lines 10-12. Specifically, there is an unclear wording within limitation in lines 6-7 "said first Q shifter shifting said **first product an instruction** specified number of bits responsive to the rounding dot product instruction" since the instruction specified number of bits

responsive to the rounding dot product instruction is not related to the first Q shifter shifting said first product, similar for limitation in lines 10-12.

Claims 13 and 25-29 were rejected under 35 U.S.C. 101 as directed to non-statutory subject matter.

The applicant argues extensively in pages 7-14 generally for claims 13 and 25-29 rejected under 35 U.S.C. 101 that the claims are system and apparatus directed to a special-purpose microprocessor as special hardware for performing a specific function with a greater performance than a general-purpose microprocessor, such as IDCT.

Upon extensive reconsider of the claimed invention and the applicant's argument, the examiner believes these claims 13 and 25-29 are directed to statutory subject matter as following reasons:

(1) These claims are directed to a special-purpose microprocessor, e.g. ASIC hardware, for performing a rounding dot product, wherein the special-purpose microprocessor is not the same as the general-purpose microprocessor as widely known and clearly stated in the specification. Basically, the microprocessor merely contains the basis hardware components (e.g. multiplier, adder, shifting, register…), but upon programming, these basis hardware components are structuralized in an unique and dedicated way according to the programmed instructions to become a special-purpose microprocessor. These special-purpose microprocessors are designed to perform a specific task (e.g. rounding dot product, IIR, FIR, or any other special function) by dedicating the basis hardware components with greater performance. These special-

purpose microprocessors might refer as application-specific integrated circuit (e.g. ASIC).

(2) These claims are not purely math or abstract idea since the claims direct to a physical special-purpose microprocessor comprising several basis hardware components for performing the rounding dot product instruction.

(3) These claims are not preemptively covered every substantial practical applications as previously mention since there are many other distinct way/methods capable of performing the claimed rounding dot product. As evidence, the mid-position rounding in the claimed dot product could be carried out in other manners such as using two circuits in cascade or by two sequential operations, instead of using a single adder/subtractor for performing addition and rounding at mid-position as cited in the claimed invention.

Therefore, the rejection under 35 U.S.C. 101 of claims 13 and 25-29 have been fully reconsidered and withdrawn.

B. Claim 13 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al. (U.S. Patent No. 6,167,419) and Pitsianis et al. (U.S. Patent Application Publication No. 2003/0088601).

The applicant argues in page 15 first paragraph for claim 13 rejected under 35 U.S.C. 103(a) that the cited primary reference by Saishi et al. does not disclose the claimed adder/subtractor circuit since the adder/subtractor circuit 506-508 in Figure 5 is part of the multiplication means for producing the product of multiplier.

The examiner respectfully submits that the claimed adder/subtractor circuit can be clearly seen in any Figures 1-5 by the cited primary reference Saishi et al. wherein Figure 1 discloses the claimed adder/subtractor circuit as addition means 109; Figure 2 discloses the claimed adder/subtractor circuit as additional means 209; Figure 3 discloses the claimed adder/subtractor circuit as components 306-308; Figure 4 discloses the claimed adder/subtractor circuit as components 406-408; and finally Figure 5 discloses the claimed adder/subtractor circuit as components 506-508. As specific by the Figures and description, the multiplication means is not a multiplier only but the multiplication means composes the multiplication stage and the addition stage. Wherein the multiplication stage 504 in Figure 5 is intended as multiplier for generating plurality of subproducts and the addition stage 506-508 in Figure 5 is intended as addition/subtraction for adding the plurality subproducts 505 (e.g. output of component 504) and mid-rounding (e.g. by the rounding signal 514) to product the final mid-rounding product of the plurality of subproducts. Thus, the examiner believes that any Figures 1-5 within the cited reference by Saishi et al. disclose the above alleged limitations, particularly Figure 5.

The applicant argues in page 15 last paragraph to first paragraph of page 16 for claim 13 that the combination of references by Saishi et al. and Pitsianis et al. does not disclose the claimed invention since the secondary reference by Pitsianis et al. discloses the production of two products but does not disclose a single adder/subtractor circuit combining these two products and rounding as recited in claim 13.

The examiner respectfully submits and acknowledged that the secondary reference by Pitsianis et al. alone does not disclose the exact claimed invention as argued by the applicant above. In addition, the examiner has never admitted or stated that the secondary reference by Pitsianis et al. discloses all the features/limitations cited in the claimed invention. Rather, the examiner only borrows and applies a dot product instruction concept from the secondary reference by Pitsianis et al. into the primary reference by Saishi et al. in order to derive/form a logical, reasonable, and obvious final claimed invention. The missing feature/limitation in the primary reference by Saishi et al., "the dot product instruction for multiplying multiple pairs of elements", is clearly found in the secondary reference by Pitsianis et al., particularly Figures 3B and 6. Thus, the secondary reference by Pitsianis et al. does not necessary to show/disclose others features/limitations as alleged by the applicant (i.e. otherwise the secondary reference can be the primary reference alone since it discloses all the limitations of the claimed invention).

In general, the primary reference by Saishi et al. discloses a single set of operand multiplication with rounding processes as recited in the claim wherein the secondary reference is combined to disclose a plurality set of operands multiplication. Thus, the combination of references clearly disclose a plurality multiplication of sets of operands (e.g. more than one multiplication or product) and a single adder/subtractor circuit (e.g. adder circuit) is used to add all the products (e.g. produce by multipliers) with a rounding signal to yield a sum rounded of products as cited in the claims. The single adder/subtractor circuit of the claimed invention is the adder means 506-508 in the

primary reference Figure 5 wherein this single adder means will sum all the outputs from multipliers (e.g. as subproducts and from secondary reference) along with a rounding signal 515 in Figure 5 at appropriated place for rounding at mid-position. Therefore, the primary reference discloses a combination of a single product and rounding in a single adder/subtractor circuit wherein the secondary reference discloses a combination of two products.

The applicant argues in pages 16-18 for claim 13 rejected under 35 U.S.C. 103(a) that the primary reference by Saishi et al. fails to disclose the adder/subtractor circuit includes "a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction".

The examiner respectfully submits that the current language does not clearly address when (e.g. before the multiplication, during the multiplication, or after the multiplication) the predetermined bit is determined for adding or inserting a carry input bit. Thus as long as a carry bit is appropriately added to mid-position of result, it meets the limitations cited in the claim. Further, the position to add the carry bit in the primary reference is not randomly determined but rather it is either algorithm/desired determined/calculated right before the adding process. The paragraph in column 8 lines 27-40 with support of Figure 8 clearly indicated a mid-position rounding wherein the predetermined rounding position 811 (e.g. lines 29-30 in column 8) is located at the mth bit wherein the kth bit can be set at 0. Generally by having or setting the (m+k)-th bit as m-th bit (e.g. k = 0) in Figure 8, then the rounding will occur at the mid-position.

C. Claims 25-27 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al. (U.S. Patent No. 6,167,419) and Peleg et al. (U.S. Patent No. 6,385,634).

The applicant argues in page 19 first paragraph for claim 25 rejected under 35 U.S.C. 103(a) that the primary reference by Saishi et al. fails to disclose the adder/subtractor circuit having a first and second inputs and a mid-position carry input as cited in the claimed invention since the adder/subtractor circuit 506-508 in Figure 5 is part of the multiplication means for producing the product of multiplier.

The examiner respectfully submits that the claimed adder/subtractor circuit can be clearly seen in any Figures 3-5 by the cited primary reference Saishi et al. wherein Figure 3 discloses the claimed adder/subtractor circuit as components 306-308; Figure 4 discloses the claimed adder/subtractor circuit as components 406-408; and finally Figure 5 discloses the claimed adder/subtractor circuit as components 506-508. Each adder/subtractor circuit of the Figures 3-5 receives multiple inputs (e.g. as subproducts input) and a mid-position carry input (e.g. as rounding signal at a predetermined position). As specific by the Figures and description, the multiplication means is not a multiplier only but the multiplication means composes the multiplication stage and the addition stage. Wherein the multiplication stage 504 in Figure 5 is intended as multiplier for generating plurality of subproducts and the addition stage 506-508 in Figure 5 is intended as addition/subtraction for adding the plurality subproducts 505 (e.g. output of component 504) and mid-rounding (e.g. by the rounding signal 514) to product the final

mid-rounding product of the plurality of subproducts. Thus, the examiner believes that any Figures 1-5 within the cited reference by Saishi et al. disclose the above alleged limitations, particularly Figure 5.

The applicant argues in page 20 second paragraph for claim 25 that the combination of references by Saishi et al. and Peleg et al. does not disclose the claimed invention since the secondary reference by Peleg et al. discloses the production of two products but does not disclose a single adder/subtractor circuit combining these two products and rounding as recited in claim 25.

The examiner respectfully submits and acknowledged that the secondary reference by Peleg et al. alone does not disclose the exact claimed invention as argued by the applicant above. In addition, the examiner has never admitted or stated that the secondary reference by Peleg et al. discloses all the features/limitations cited in the claimed invention. Rather, the examiner only borrows and applies a dot product instruction concept from the secondary reference by Peleg et al. into the primary reference by Saishi et al. in order to derive/form a logical, reasonable, and obvious final claimed invention. The missing feature/limitation in the primary reference by Saishi et al., "the dot product instruction for multiplying multiple pairs of elements", is clearly found in the secondary reference by Peleg et al., particularly Figures 1 and 8. Thus, the secondary reference by Peleg et al. does not necessary to show/disclose others features/limitations as alleged by the applicant (i.e. otherwise the secondary reference can

be the primary reference alone since it discloses all the limitations of the claimed invention).

In general, the primary reference by Saishi et al. discloses a single set of operand multiplication with rounding processes as recited in the claim wherein the secondary reference is combined to disclose a plurality set of operands multiplication. Thus, the combination of references clearly disclose a plurality multiplication of sets of operands (e.g. more than one multiplication or product) and a single adder/subtractor circuit (e.g. adder circuit) is used to add all the products (e.g. produce by multipliers) with a rounding signal to yield a sum rounded of products as cited in the claims. The single adder/subtractor circuit of the claimed invention is the adder means 506-508 in the primary reference Figure 5 wherein this single adder means will sum all the outputs from multipliers (e.g. as subproducts and from secondary reference) along with a rounding signal 515 in Figure 5 at appropriated place for rounding at mid-position. Therefore, the primary reference discloses a combination of a single product and rounding in a single adder/subtractor circuit wherein the secondary reference discloses a combination of two products.

The applicant argues in pages 20-22 for claim 25 rejected under 35 U.S.C. 103(a) that the primary reference by Saishi et al. fails to disclose the adder/subtractor circuit includes "a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction" wherein this operation normally requiring two hardware circuits to perform.

The examiner respectfully submits that the current language does not clearly address when (e.g. before the multiplication, during the multiplication, or after the multiplication) the predetermined bit is determined for adding or inserting a carry input bit. Thus as long as a carry bit is appropriately added to mid-position of result, it meets the limitations cited in the claim. Further, the position to add the carry bit in the primary reference is not randomly determined but rather it is either algorithm/desired determined/calculated right before the adding process. The paragraph in column 8 lines 27-40 with support of Figure 8 clearly indicated a mid-position rounding wherein the predetermined rounding position 811 (e.g. lines 29-30 in column 8) is located at the mth bit wherein the kth bit can be set at 0. Generally by having or setting the (m+k)-th bit as m-th bit (e.g. k = 0) in Figure 8, then the rounding will occur at the mid-position.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Chat C. Do/

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